Appl. No.: 10/766,971
Amdt. dated September 6, 2005
Reply to Office Action of July 7, 2005

Admendments to the Claims:

The below listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A structure package comprising:

a first semiconductor chip having a first integrated circuit;

a substrate having a first electrically conductive pattern formed thereon, the first electrically conductive pattern being an antenna layer; and

a plurality of pillars, at least one of the plurality of pillars extending from the first semiconductor chip to the substrate for structurally intercoupling and spatially interdisplacing the first semiconductor chip and the substrate for forming a first channel therebetween,

wherein at least one of the plurality of pillars is for electrically communicating the first integrated circuit with the first electrically conductive pattern.

2. (Currently Amended) The structure package as in claim 1, ~~the first electrically conductive pattern being an antenna layer and~~ the integrated circuit being a data transceiver circuit in operative communication with the first electrically conductive pattern.

3. (Currently Amended) The structure package as in claim ~~1~~ 2, further comprising:

a second electrically conductive pattern, the first electrically conductive pattern and the second electrically conductive pattern being formed on two outwardly opposing faces of the substrate,

wherein at least one of the plurality of pillars is for electrically communicating the integrated circuit with the second electrically conductive pattern.

4. (Currently Amended) The structure package as in claim 3, ~~at least one of the first electrically conductive pattern and~~ the second electrically conductive pattern being an antenna layer and the integrated circuit being ~~a data transceiver circuit~~ in operative

communication with ~~at least one of the first electrically conductive pattern and~~ the second electrically conductive pattern.

5. (Original) The structure package as in claim 4, the first electrically conductive pattern and the second electrically conductive pattern are for transmitting and receiving data signals.

6. (Currently Amended) The structure package as in claim ~~1~~ 2, further comprising:

at least one inter-connector formed through the substrate and the first electrically conductive pattern, the inter-connector for electrically connecting the second electrically conductive pattern to one of the plurality of pillars to thereby electrically inter-communicate the second electrically conductive pattern with the integrated circuit,

wherein the at least one inter-connector is one of electrically insulated from and in electrical communication with the first electrically conductive pattern.

7. (Currently Amended) The structure package as in claim ~~1~~ 2, the first semiconductor chip and the substrate being arranged in a stacked configuration for forming the first channel between the substrate and the first semiconductor chip.

8. (Original) The structure package as in claim 7, the first channel being filled with a filler material.

9. (Currently Amended) The structure package as in claim ~~1~~ 2, a portion of the plurality of pillars being spaced apart along the substrate when being disposed between the substrate and the first semiconductor chip.

10. (Currently Amended) The structure package as in claim ~~1~~ 2, at least one of the plurality of pillars being formed from at least two conductive materials.

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11. (Original) The structure package as in claim 10, one of the at least two conductive material being solder material.

12. (Currently Amended) The structure package as in claim ~~1~~ 2, at least one pair of the plurality of pillars having dielectric material extending therebetween.

13. (Original) The structure package as in claim 12, the dielectric material being one of low-K dielectric material and high-K dielectric material.

14. (Currently Amended) The structure package as in claim ~~1~~ 2, each of at least a portion of the plurality of pillars being formed abutting at least another one of the plurality of pillars along the substrate for enclosing a shielded space between the substrate and the first semiconductor chip, the shielded space for electrically shielding at least one of at least a portion of the first integrated circuit of the first semiconductor chip and at least a portion of the first electrically conductive pattern formed on the substrate.

15. (Currently Amended) The structure package as in claim ~~1~~ 2, the first integrated circuit comprising an antenna.

16. (Original) The structure package as in claim 15, the first electrically conductive pattern being at least a portion of a data transceiver circuit.

17. (Currently Amended) The structure package as in claim ~~1~~ 2, further comprising:

a second semiconductor chip having a second integrated circuit, at least one of the plurality of pillars extending from the second semiconductor chip to and spatially displacing the second semiconductor chip from one of the first semiconductor chip and the substrate,

wherein at least one of the plurality of pillars is for electrically communicating the second integrated circuit with at least one of the first integrated circuit and the first electrically conductive pattern.

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18. (Original) The structure package as in claim 17, the first electrically conductive pattern being at least a portion of a data transceiver circuit and each of the first integrated circuit and the second integrated circuit comprising an antenna.

19. (Original) The structure package as in claim 17, the first semiconductor chip, the second semiconductor chip and the substrate being arranged in a stacked configuration with a second channel being formed between the second semiconductor chip and the first semiconductor chip.

20. (Original) The structure package as in claim 16, the second channel being filled with a filler material.

21. (Original) A data transceiver for transceiving data signals comprising:

a first semiconductor chip having a data transceiver circuit;

a substrate having a first antenna pattern formed thereon; and

a plurality of pillars, at least one of the plurality of pillars extending from the first semiconductor chip to the substrate for structurally intercoupling and spatially interdisplacing the first semiconductor chip and the substrate for forming a first channel therebetween,

wherein at least one of the plurality of pillars is for electrically connecting and operatively communicating the data transceiver circuit with the first antenna pattern.

22. (Original) The data transceiver as in claim 21, further comprising:

a second antenna pattern, the antenna pattern and the second antenna pattern being formed on two outwardly opposing faces of the substrate,

wherein at least one of the plurality of pillars is for electrically connecting and operatively communicating the data transceiver circuit with the second antenna pattern.

23. (Original) The data transceiver as in claim 22, the first antenna pattern and the second antenna pattern are for transmitting and receiving data signals.

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24. (Original) The data transceiver as in claim 22, further comprising:

at least one inter-connector formed through the substrate and the first antenna pattern, the inter-connector for electrically connecting the second antenna pattern to one of the plurality of pillars to thereby electrically inter-communicate the second antenna pattern with the data transceiver circuit,

wherein the at least one inter-connector is one of electrically insulated from and in electrical communication with the first antenna pattern.

25. (Currently Amended) The data transceiver as in claim ~~21~~ 22, the first semiconductor chip and the substrate being arranged in a stacked configuration for forming the first channel between the substrate and the first semiconductor chip.

26. (Original) A data transceiver for transceiving data signals comprising:

a first semiconductor chip having a first integrated circuit, the first integrated circuit comprising an antenna;

a substrate having a data transceiver circuit formed thereon; and

a plurality of pillars, at least one of the plurality of pillars extending from the first semiconductor chip to the substrate for structurally intercoupling and spatially interdisplacing the first semiconductor chip and the substrate for forming a first channel therebetween,

wherein at least one of the plurality of pillars is for electrically communicating the first integrated circuit with the data transceiver circuit.

~~27~~ 30. (Currently Amended) The data transceiver as in claim ~~26~~ 27, a portion of the plurality of pillars being spaced apart along the substrate when being disposed between the substrate and the first semiconductor chip.

28. (Currently Amended) The data transceiver as in claim ~~26~~ 27, further comprising:

a second semiconductor chip having a second integrated circuit, the second integrated circuit comprising antenna, at least one of the plurality of pillars extending

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from the second semiconductor chip to and spatially displacing the second semiconductor chip from the first semiconductor chip,

wherein at least one of the plurality of pillars is for electrically communicating the second integrated circuit with at least one of the first integrated circuit and the first data transceiver circuit.

29. (Original) The data transceiver as in claim 28, the first semiconductor chip, the second semiconductor chip and the substrate being arranged in a stacked configuration with a second channel being formed between the second semiconductor chip and the first semiconductor chip.

~~30~~ 27. (Currently Amended) The data transceiver as in claim 26, each of at least a portion of the plurality of pillars being formed abutting at least another one of the plurality of pillars along the substrate for enclosing a shielded space between the substrate and the first semiconductor chip, the shielded space for electrically shielding at least one of at least a portion of the first integrated circuit of the first semiconductor chip and at least a portion of the data transceiver circuit formed on the substrate.

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